Single-Channel 1.1A USB High-Side Power Switch with Flag

Description

The FP6861 is a single channel USB power switch which is optimized for the self-powered and the bus-powered Universal Serial Bus (USB) applications. It is cost-effective, low voltage and equipped single N-Channel high-side MOSFET switch.

For driving the internal MOSFET switch, a charge pump circuitry is built in the FP6861. The switch's low $R_{DS(ON)}$, 95mΩ, meets USB voltage drop requirement, and a fault flag output is available to indicate fault conditions to the local USB controller.

Other additional features include under-voltage lockout (UVLO) to ensure that the device keeps off until input a valid voltage, thermal shutdown to prevent catastrophic switch failure from high loading current and fault current is limited to typically 1.5A for in accordance with the USB power requirements. Soft-start to limit inrush current during plug-in and lower quiescent current as 33μA making this device ideal for portable battery-operated equipment.

The FP6861 is available in SOT-23-5 package requiring minimum board space and smallest components.

Features

- Guaranteed 1.1A Continuous Load Current
- Input Voltage Ranges : 2V to 5.5V
- Open-Drain Fault Flag Output
- Built-In N-Channel MOSFET : Typically 95mΩ
- Output Can Be Forced Higher Than Input (Off-State)
- 1.7V Typical Under-Voltage Lockout (UVLO)
- Low Supply Current :
  33μA Typical at Switch On State
  0.1μA Typical at Switch Off State
- Hot Plug-In Application (Soft-Start)
- Current Limiting Protection
- Thermal Shutdown Protection
- Reverse Current Flow Blocking (No Body Diode)
- Logic Level Enable Pin, Available with Active High and Active-Low Versions
- RoHS Compliant
- UL Approved -E322418

Applications

- Notebook PCs
- LCD Monitors
- USB Bus/Self Powered Hubs
- USB Peripherals
- ACPI Power Distribution

Pin Assignments

S5 Package (SOT-23-5)

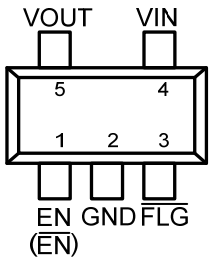


Figure 1. Pin Assignment of FP6861

Ordering Information

FP6861□□□□

- TR: Tape / Reel
- P: Green
  G: Green
- Blank: Active High
  L: Active Low
- Package Type
  S5: SOT-23-5

SOT-23-5 Marking

Part Number	Product Code	Part Number	Product
FP6861S5P	J1	FP6861S5LG	T9=
FP6861S5G	J1=		

Typical Application Circuit

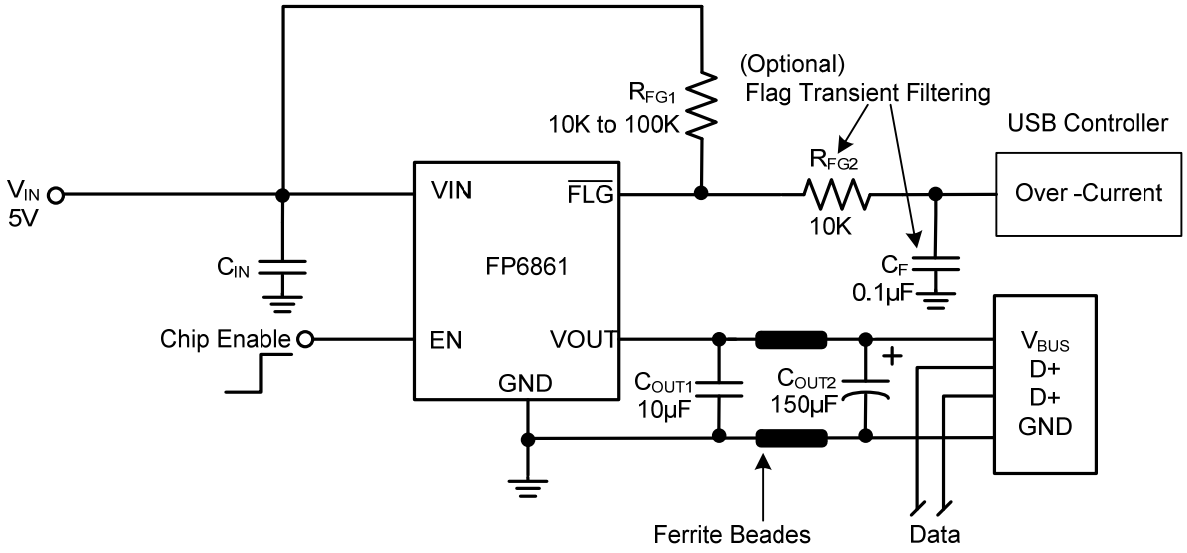


Figure 2. Typical Application Circuit of FP6861

Functional Pin Description

Pin Name	Pin Function
VIN	Input Power Supply
VOUT	Switch Output
GND	Ground
EN	Chip Enable. Pull the pin high to enable IC; Pull the pin low to shutdown IC. Do not let the pin floating.
$\overline{\text{EN}}$	Chip Shutdown. Pull the pin high to shutdown IC; Pull the pin low to enable IC. Do not let the pin floating.
$\overline{\text{FLG}}$	Open-Drain Fault Flag Output

Block Diagram

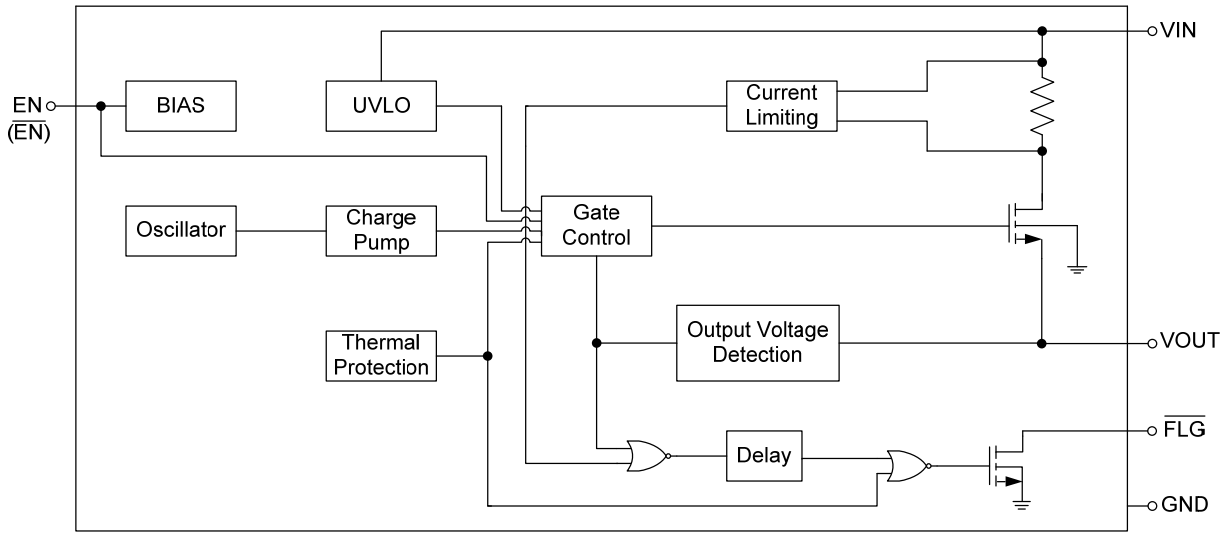


Figure 3. Block Diagram of FP6861

Absolute Maximum Ratings

- VIN, VOUT---------- -0.3V to 6V
- EN (/EN)---------- -0.3V to 6V
- /FLG---------- -0.3V to 6V
- Power dissipation @T_A=25℃, SOT-23-5 (P_D) ---------- 0.4W
- Package Thermal Resistance, SOT-23-5 (θ_{JA})---------- 250°C/W
- Maximum Junction Temperature (T_J)---------- +150℃
- Lead Temperature (Soldering, 10 sec.)---------- 260℃
- Storage Temperature Range (T_{STG})---------- -65℃ to +130℃

Note1：Stresses beyond those listed under “Absolute Maximum Ratings" may cause permanent damage to the device.

Recommended Operating Conditions

- Supply Voltage (V_{IN})---------- +2V to + 5.5V
- Operation Temperature Range (T_{OPR})---------- -40°C to +85°C

Electrical Characteristics

(V_{IN}=5V, C_{IN}=C_{OUT}=1μF, T_A=25℃, unless otherwise specified.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Switch On Resistance (Note2)	$R_{DS(ON)}$	I_{OUT}=1.1A		95		mΩ
Supply Current	I_{SW_ON}	Switch on, V_{OUT} = Open		33		μA
	I_{SW_OFF}	Switch off, V_{OUT} = Open		0.1	1	
EN Threshold	V_{IL}	Logic Low			0.8	V
	V_{IH}	Logic High	2.0			
EN Input Current	I_{EN}	V_{EN} = 0V to 5.5V		0.01	1	μA
Output Leakage Current	$I_{LEAKAGE}$	V_{EN} = 0V, R_{LOAD} = 0Ω		0.5	5	μA
Output Turn-On Rise Time	T_{ON_RISE}	10% to 90% of V_{OUT} rising		330		μs
Current Limit	I_{LIM}	R_{LOAD} = 1Ω	1.1	1.5	2.0	A
Short Circuit Fold-Back Current	I_{SC_FB}	V_{OUT} = 0V, measured prior to thermal shutdown		1.0		A
/FLG Output Resistance	$R_{\overline{FLG}}$	I_{SINK} = 1mA		20	400	Ω
/FLAG Off Current	$I_{\overline{FLG}\_OFF}$	$V_{\overline{FLG}}$ = 5V		0.01	1	μA
FLAG Delay Time	t_D	From fault condition to $\overline{FLG}$ assertion		60		ms
Under Voltage Lockout	V_{UVLO}	V_{IN} increasing	1.3	1.7		V
Under Voltage Hysteresis	ΔV_{UVLO}	V_{IN} decreasing		0.1		V
Thermal Shutdown Threshold (Note2)	T_{SD}			160		℃
	ΔT_{SD}	Hysteresis		30		℃

Note2: Guarantee by design.

Test Circuit

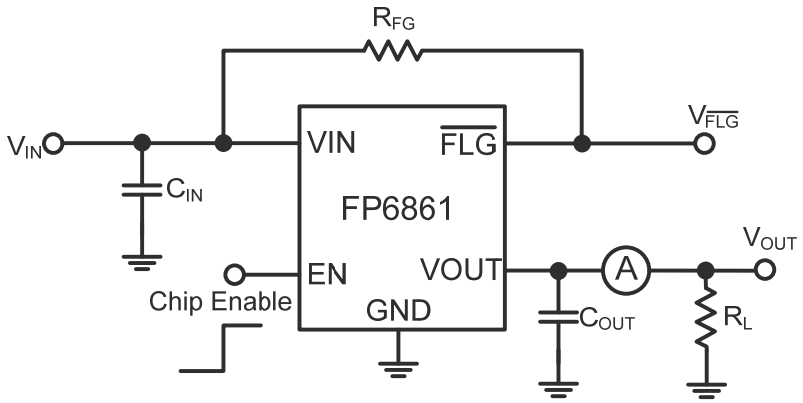


Figure 4.Electrical Characteristic Test Circuit of FP6861

Typical Performance Curves

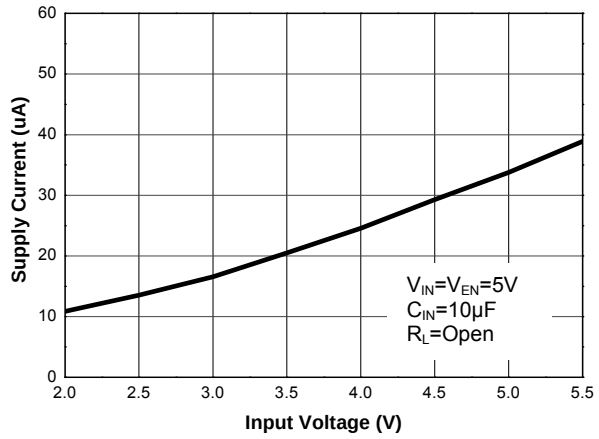


Figure 5. Supply Current vs. Input Voltage

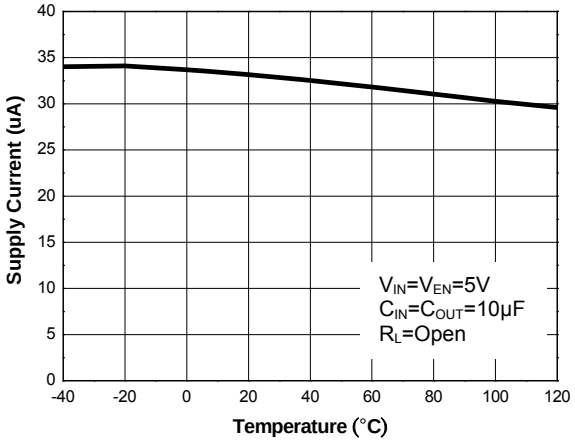


Figure 6. Supply Current vs. Temperature

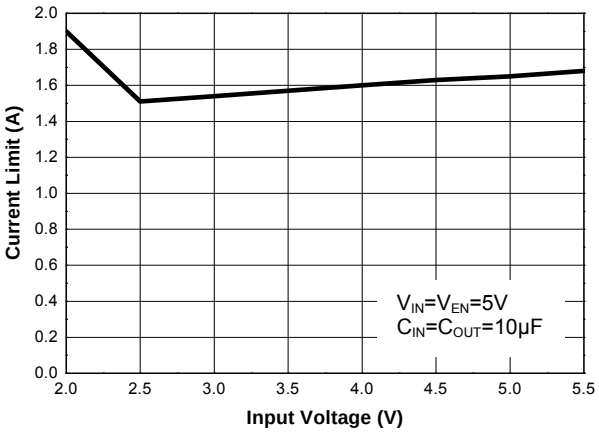


Figure 7.Current Limit vs. Input Voltage

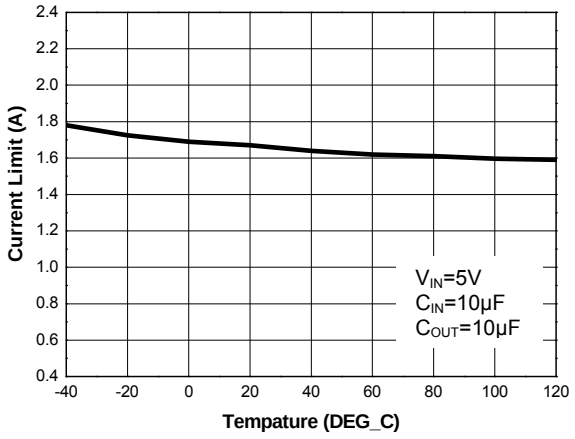


Figure 8.Current Limit vs. Temperature

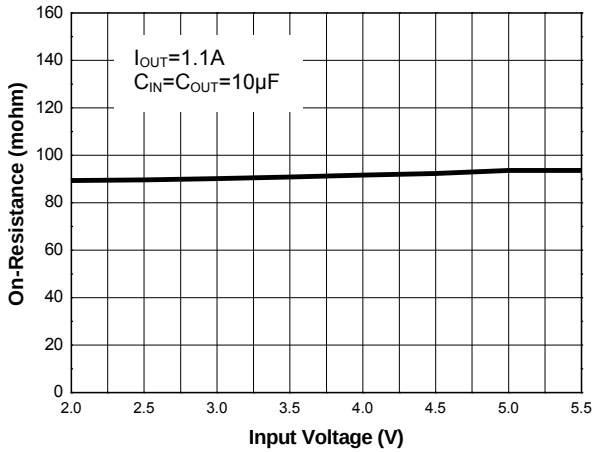


Figure 9.On-Resistance vs. Input Voltage

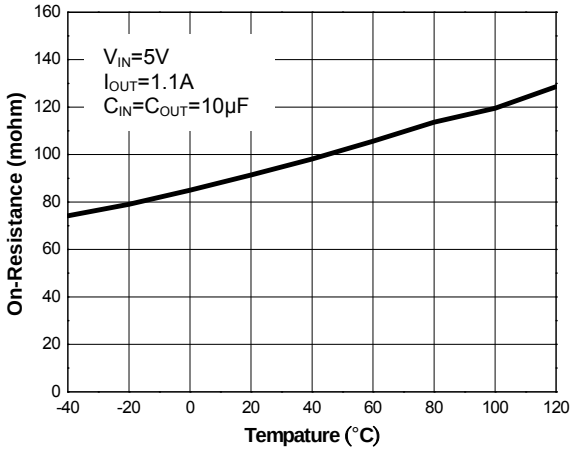


Figure 10.On-Resistance vs. Temperature

Typical Performance Curves (Continued)

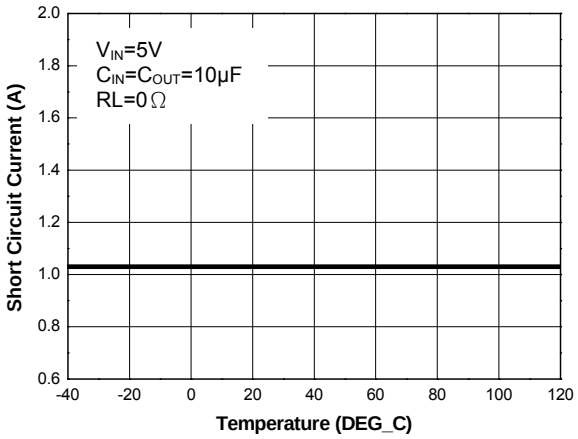


Figure 11.Short Circuit Current vs. Temperature

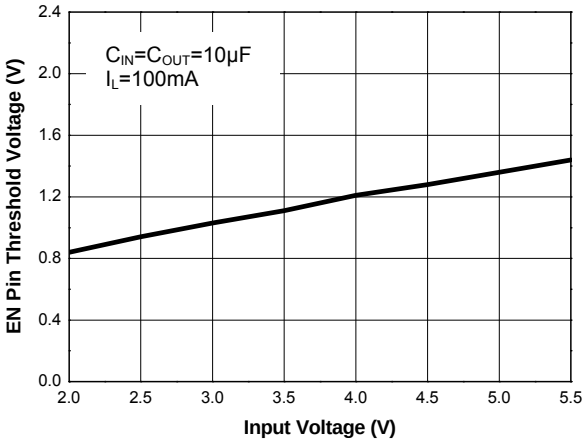


Figure 12.EN Pin Threshold Voltage vs. Input Voltage

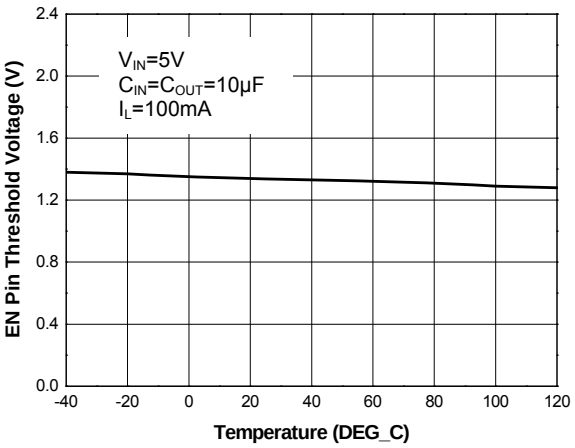


Figure 13.EN Pin Threshold Voltage vs. Temperature

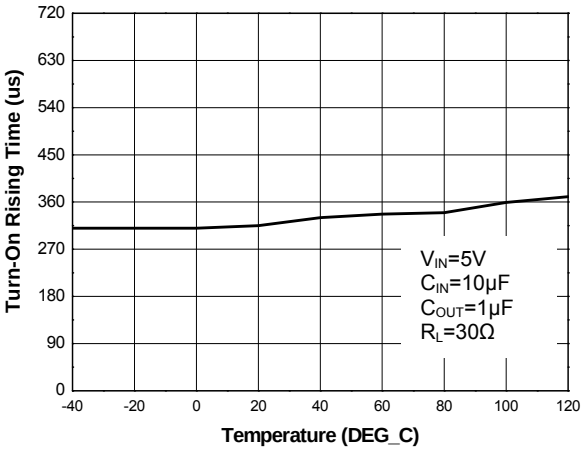


Figure 14.Turn-On Rising Time vs. Temperature

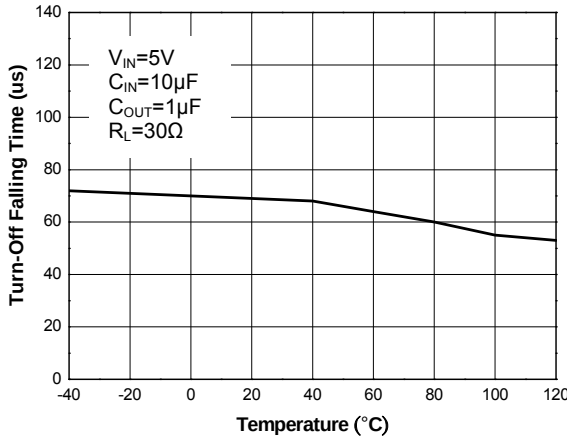


Figure 15.Turn-Off Falling Time vs. Temperature

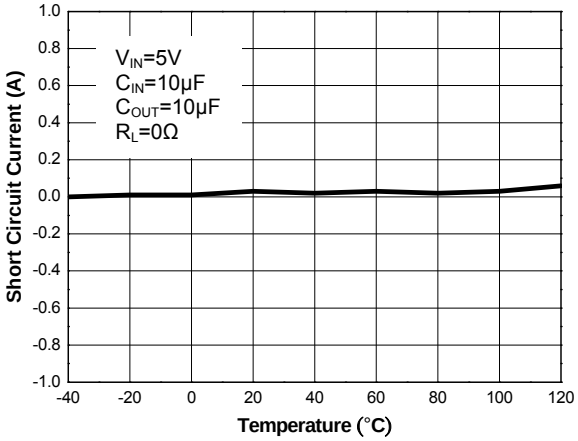


Figure 16.Switch Off Supply Current vs. Temperature

Typical Performance Curves (Continued)

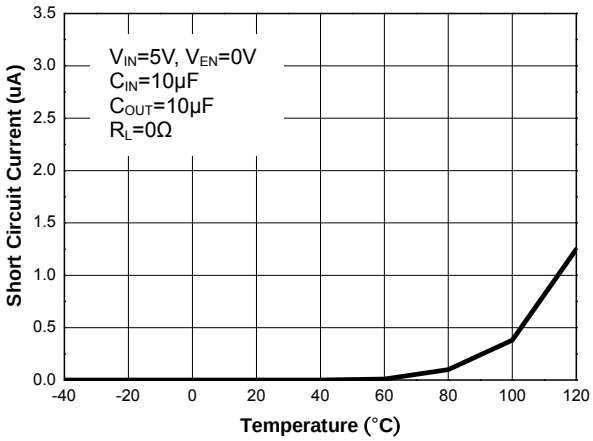


Figure 17.Turn-off Leakage Current vs. Temperature

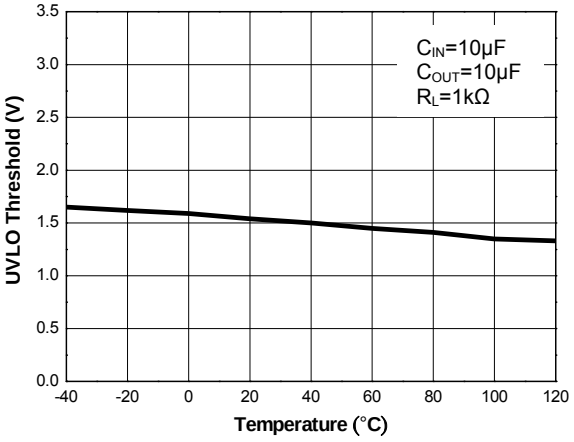


Figure 18.UVLO Threshold vs. Temperature

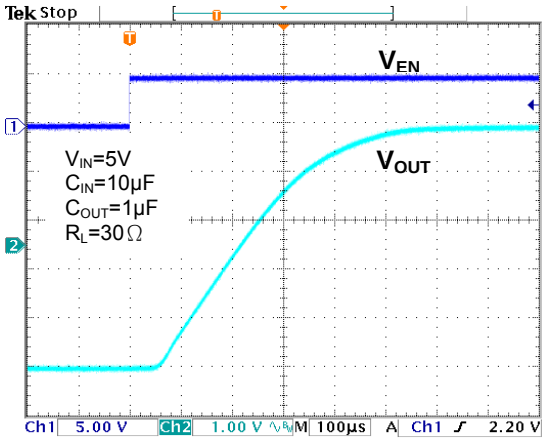


Figure 19.Turn-On Response

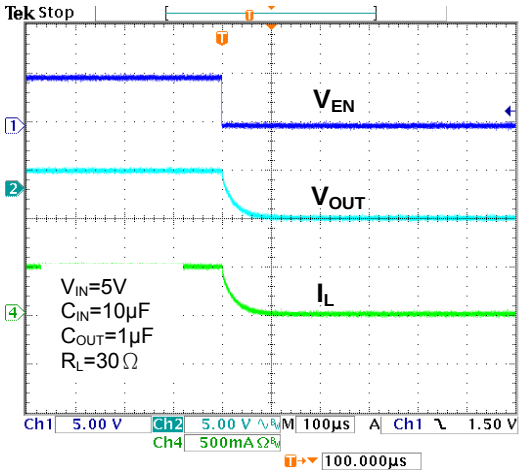


Figure 20.Turn-off Response

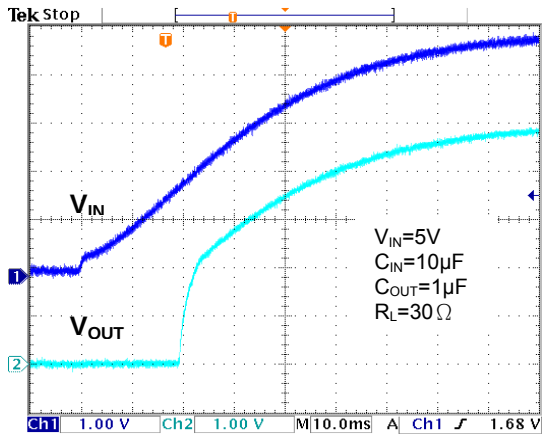


Figure 21. UVLO at Rising

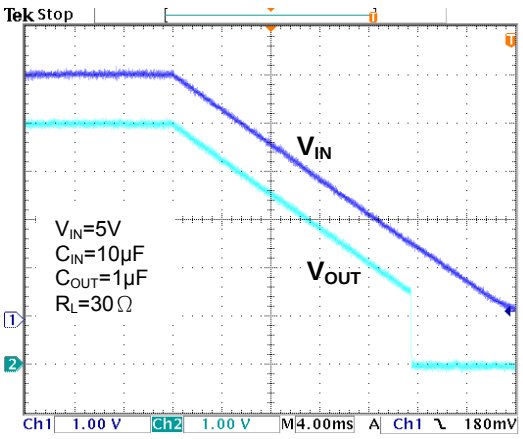


Figure 22.UVLO at Falling

Typical Performance Curves (Continued)

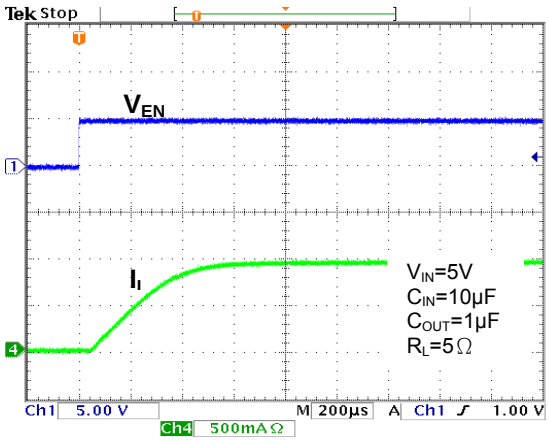


Figure 23. Soft Start Response

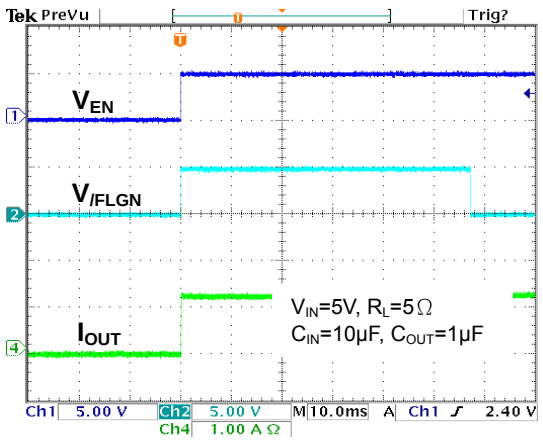


Figure 24.Flag Response

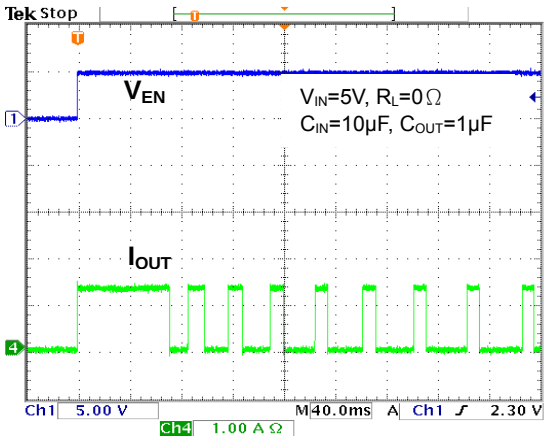


Figure 25.Short Circuit Thermal Shutdown Response

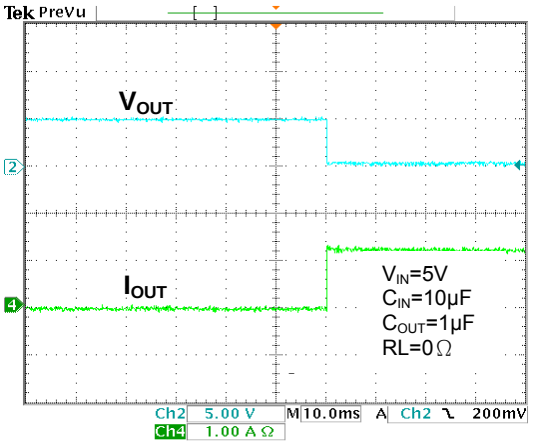


Figure 26.Short Circuit Current Response

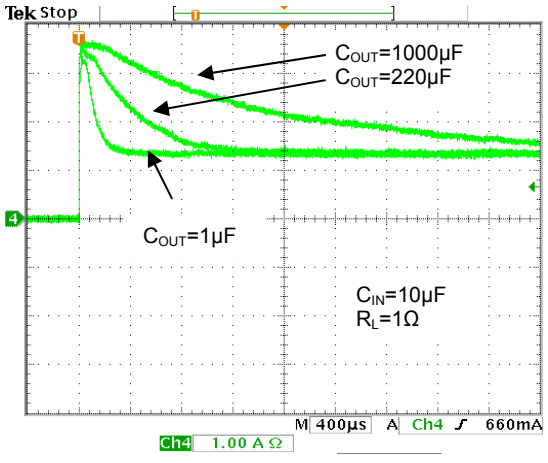


Figure 27. Short Circuit Current Response

Functional Description

The FP6861 is a single, current-limited switch designed for USB applications. The FP6861 operates from 2.0V to 5.5V input voltage range and guarantees a minimum 1.1A output current. It has one switch with enable control input. The switch has an error flag output to notify the USB controller when the current-limit, short-circuit, under-voltage-lockout or thermal-shutdown occurs.

1. Under Voltage-Lockout

Under voltage-lockout (UVLO) circuit prevents the output switch from turning on until input voltage exceeds approximately 1.7V.

2. Thermal Shutdown

Thermal shutdown is employed to protect the device from damage if the die temperature exceeds safe margins due mainly to short-circuit or current-limit. Thermal shutdown shuts the switch off when current-limit or short-circuit occur and asserts the /FLG output if the die temperature reaches 160 ºC.

3. Reverse Current Blocking

The USB specification does not allow an output device to source current back into the USB port. However, the FP6861 is designed to safely power noncompliant devices. When disable, the output is switched to a high-impedance state, blocking reverse current flow from the output back to the input. The switch is bidirectional when enable.

4. Error Flag

The FP6861 provides an open drain error flag output for the switch. For most applications, connect /FLG to V_{IN} through a pull-up resistor. /FLG goes low when any following condition occurs:

a. The input voltage is below the UVLO threshold.

b. The thermal shutdown occurs.

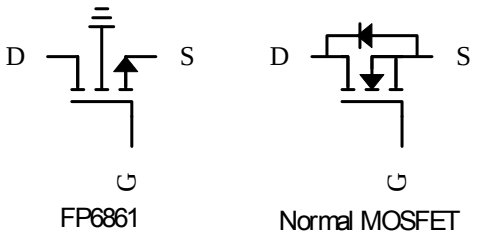
c. The switch is in current limit or short circuit conditions.

Application Information

The FP6861 is a single N-Channel MOSFET high-side power switch with active high or low enable input, optimized for self-powered and bus-powered Universal Serial Bus (USB) applications. The FP6861 is designed with a charge pump circuitry to drive the internal NMOS switch; the switch's low $R_{DS(ON)}$, 95mΩ, meets USB voltage drop requirements; and the flag output is available to indicate fault conditions to the USB controller.

Input and Output

VIN is the power source connection to the internal circuitry and the drain of the MOSFET. VOUT is the source of the MOSFET. In typical application, current flows through the switch from VIN to VOUT toward the load. If VOUT is greater than VIN, current will flow from VOUT to VIN since the MOSFET is bidirectional. There is no a parasitic body diode between drain and source of the MOSFET, the FP6861 prevents reverse current flow if VOUT externally forced a higher voltage than VIN when the output disabled (V_{EN} < 0.8V).



Chip Enable Input

EN must be driven logic high or low for a clearly defined input. Floating the input may cause unpredictable operation.

Soft Start for Hot Plug-In Application

In order to eliminate the upstream voltage droop caused by the large inrush current during hot-plug events, the “soft-start” feature effectively isolates the power source from extremely large capacitive loads, satisfying the USB voltage droop requirements.

Application Information (Continued)

Fault Flag

The FP6186 provides a /FLG signal pin which is an N-Channel open drain MOSFET output. This open drain output goes low when V_{OUT} < V_{IN}-1V, current limit or the die temperature exceeds 160°C approximately. The /FLG output is capable of sinking a 10mA load to typically 200mV above ground. The /FLG pin requires a pull-up resistor; this resistor should be large in value to reduce energy drain. A 100kΩpull-up resistor works well for most applications. In the case of an over-current condition, /FLG will be asserted only after the 60ms flag response delay time. This ensures that /FLG is asserted only upon valid over-current conditions and that erroneous error reporting is eliminated.

For example, false over-current conditions may occur during hot-plug events when extremely large capacitive loads are connected and causes a high transient inrush current that exceeds the current limit threshold.

UVLO Under-Voltage Lockout

Under-voltage lockout (UVLO) prevents the MOSFET switch from turning on until input voltage exceeds approximately 1.7V. If input voltage drops below approximately 1.6V, UVLO turns off the MOSFET switch, /FLG will be asserted accordingly.

Current Limiting and Short-Circuit Protection

The current limit circuitry prevents damage to the MOSFET switch and the hub downstream port but can deliver load current up to the current limit threshold of typically 1.5A through the switch of FP6861. When a heavy load or short circuit is applied to an enabled switch, a large transient current may flow until the current limit circuitry responds. Once this current limit threshold is exceeded the device enters constant current mode until the thermal shutdown occurs or the fault is removed.

Thermal Shutdown

Thermal shutdown is employed to protect the device from damage if the die temperature exceeds approximately 160°C.

The power switch will auto-recover when the IC is cooling down. The thermal hysteresis temperature is about 30°C.

Power Dissipation

The device's junction temperature depends on several factors such as the load, PCB layout, ambient temperature and package type. The output pin of FP6861 can deliver a current up to 1.1A, respectively over the full operating junction temperature range. However, the maximum output current must be decreased at higher ambient temperature to ensure the junction temperature does not exceed 160°C. With all possible conditions, the junction temperature must be within the range specified under operating conditions. Power dissipation can be calculated based on the output current and the $R_{DS(ON)}$ of switch as below.

$$P_D = R_{DS(ON)} \times (I_{OUT})^2$$

Although the devices are rated for 1.1A of output current, but the application may limit the amount of output current based on the total power dissipation and the ambient temperature. The final operating junction temperature for any set of conditions can be estimated by the following thermal equation :

$$P_{D\,(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

Where $T_{J(MAX)}$ is the maximum operation junction temperature 125°C, T_A is the ambient temperature and the θ_{JA} is the junction to ambient thermal resistance.

The junction to ambient thermal resistance θ_{JA} is layout dependent. For SOT-23-5 packages, the thermal resistance θ_{JA} is 250°C/W on the standard JEDEC 51-3 single-layer thermal test board.

Application Information (Continued)

Supply Filter/Bypass Capacitor

A 10uF low-ESR ceramic capacitor from V_{IN} to GND, located at the device is strongly bypass capacitor, an output short may cause sufficient ringing on the input (from source lead inductance) to destroy the internal control circuitry. The input transient must not exceed 6V of the absolute maximum supply voltage even for a short duration.

Output Filter Capacitor

A low-ESR 150uF aluminum electrolytic or tantalum between V_{OUT} and GND is strongly recommended to meet the 330mV maximum droop requirement in the hub V_{BUS} (Per USB 2.0, output ports must have a minimum 120uF of low-ESR bulk capacitance per hub). Standard bypass methods should be used to minimize inductance and resistance between the bypass capacitor and the downstream connector to reduce EMI and decouple voltage droop caused when downstream cables are hot-insertion transients. Ferrite beads in series with V_{BUS}, the ground line and the 0.1uF bypass capacitors at the power connector pins are recommended for EMI and ESD protection. The bypass capacitor itself should have a low dissipation factor to allow decoupling at higher frequencies.

Voltage Drop

The USB specification states a minimum port-output voltage in two locations on the bus, 4.75V out of a Self- Powered Hub port and 4.4V out of a Bus-Powered Hub port. As with the Self-Powered Hub, all resistive voltage drops for the Bus-Powered Hub must be accounted for to guarantee voltage regulation.

The following calculation determines $V_{OUT\ (MIN)}$ for multiple ports (N_{PORTS}) ganged together through one switch (if using one switch per port, N_{PORTS} is equal to 1) :

$$V_{OUT\ (MIN)} = 4.75V - [\ I_{LOAD} \times (\ 4 \times R_{CONN} + 2 \times R_{CABLE}\ )\ ] - (0.1A \times N_{PORTS} \times R_{SWITCH}\ ) - V_{PCB}$$

where :
R_{CONN} : Resistance of connector contacts (two contacts per connector)
R_{CABLE} : Resistance of upstream cable wires (one 5V and one GND)
R_{SWITCH} : Resistance of power switch (95mΩ typical for FP6861)
V_{PCB} : PCB voltage drop

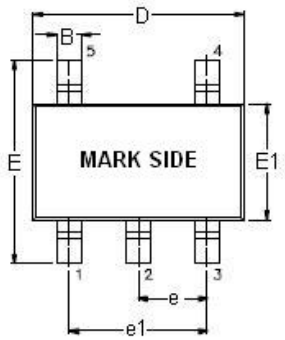
PCB Layout

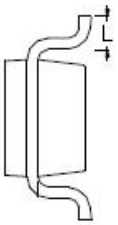
In order to meet the voltage drop, droop, and EMI requirements, careful PCB layout is necessary. The following guidelines must be considered :

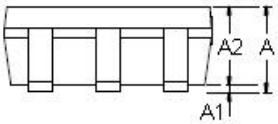
- Keep all VBUS traces as short as possible and use at least 50-mil, 2 ounce copper for all VBUS traces.
- Locate the FP6861 as close as possible to the output port to limit switching noise.
- Locate the ceramic bypass capacitors as close as possible to the V_{IN} pins of the FP6861.
- Avoid vias as much as possible. If vias are necessary, make them as large as feasible.
- Place a ground plane under all circuitry to lower both resistance and inductance and improve DC and transient performance (Use a separate ground and power plans if possible).
- Place cuts in the ground plane between ports to help reduce the coupling of transients between ports.
- Locate the output capacitor and ferrite beads as close to the USB connectors as possible to lower impedance (mainly inductance) between the port and the capacitor and improve transient load performance.

Outline Information

SOT-23-5 Package (Unit: mm)







SYMBOLS UNIT	DIMENSION IN MILLIMETER	
	MIN	MAX
A	1.00	1.20
A1	0.00	0.10
A2	1.00	1.10
B	0.35	0.50
D	2.80	3.00
E	2.60	3.00
E1	1.50	1.70
e	0.90	1.00
e1	1.80	2.00
L	0.35	0.55

Note：Followed From JEDEC MO-178-C.